

CLAIM AMENDMENTS

1 (Currently Amended). An asymmetric digital subscriber loop modem comprising:
an integrated circuit;
an analog-to-digital converter contained in said integrated circuit, said converter producing data at a relatively higher data rate;
a device contained in said integrated circuit and coupled to said analog-to-digital converter, said device reducing the higher data rate data from the analog-to-digital converter to a lower data rate data;
a multiplexer to multiplex said lower data rate data and control information and transmit said data and control information externally of said integrated circuit; and
a second integrated circuit, said second integrated circuit including a de-multiplexer to de-multiplex said lower data rate data and said control information.

Claim 2 (Canceled).

~~3~~² (Original). The modem of claim 1 wherein said device includes a decimation filter.

~~4~~³ (Currently Amended). The method of claim ~~3~~² wherein said integrated circuit includes an a analog filter coupled to said analog-to-digital converter in turn coupled to said decimation filter in turn coupled to said multiplexer.

~~5~~⁴ (Original). The modem of claim 1 wherein said integrated circuit further includes a demultiplexer coupled to a device that increases the data rate of data received by said demultiplexer, said device that increases the data rate being coupled to a digital-to-analog converter.

~~6~~⁵ (Original). The modem of claim ~~5~~⁴ wherein said device for increasing the data rate includes an interpolation filter.

~~7~~⁶ (Original). The modem of claim 1 wherein said integrated circuit includes both a receiver section and a transmitter section.

Claim 8 (Canceled).

~~9~~⁷ (Currently Amended). The modem of claim 1 8 wherein said second integrated circuit implements discrete multi-tone modulation.

~~10~~⁸ (Original). The modem of claim ~~9~~⁷ wherein said second integrated circuit provides digital signal processing.

~~11~~⁹ (Original). The modem of claim ~~9~~⁷ wherein said second integrated circuit includes a fast Fourier transformer and a line decoder.

~~12~~¹⁰ (Previously Presented). An asymmetric digital subscriber loop modem comprising:
an integrated circuit;
an analog-to-digital converter contained in said integrated circuit, said converter producing data at a relatively higher data rate;
a device contained in said circuit and coupled to said analog-to-digital converter, said device reducing the higher data rate data from the analog-to-digital converter to a lower data rate;
a multiplexer to multiplex said lower data rate data and control information and transmit said data and control information externally of said integrated circuit; and
a second integrated circuit, said second integrated circuit including a line encoder to produce data at a relatively higher data rate and a device coupled to said line encoder to produce data at a relatively lower data rate, said device being coupled to a serializer which transmits said data to said integrated circuit.

~~13~~¹¹ (Original). The modem of claim ~~12~~¹⁰ wherein said device is an inverse fast Fourier transformer.

~~14~~¹² (Previously Presented). A method comprising:
receiving analog data on a first integrated circuit device within a modem;
converting said analog data to digital format;
decreasing the data rate of said data;

serializing said data;
multiplexing said serialized data with control information;
transmitting said data to a second integrated circuit device within the modem; and
demultiplexing said data and control information within said second integrated
circuit device.

~~13~~ ¹³ (Original). The method of claim ~~14~~ ¹² wherein reducing the data rate of said digital data includes decimating said digital data.

Claim 16 (Canceled).

~~14~~ ¹⁴ (Currently Amended). The method of claim ~~14~~ ¹² ~~16~~ further including receiving said data on said second integrated circuit and de-serializing said data.

~~15~~ ¹⁵ (Original). The method of claim ~~17~~ ¹⁴ including increasing the data rate of said data on said second integrated circuit.

~~16~~ ¹⁶ (Original). The method of claim ~~18~~ ¹⁵ wherein increasing said data rate includes fast fourier transforming said data.

~~17~~ ¹⁷ (Original). The method of claim ~~14~~ ¹² further including receiving digital data for transmission by said first chip and increasing the data rate of said data.

~~18~~ ¹⁸ (Original). The method of claim ~~20~~ ¹⁷ wherein increasing said data rate includes interpolating said data.

~~19~~ ¹⁹ (Original). The method of claim ~~21~~ ¹⁸ including converting said interpolated data to an analog format signal.

~~20~~ ²⁰ (Previously Presented). An asymmetric digital subscriber loop modem comprising:
a first integrated circuit including an analog-to-digital converter, a device to
reduce the data rate from the analog-to-digital converter to a lower data rate, and a serializer to
multiplex said lower data rate data with control information; and

a second integrated circuit, said serializer to transmit said lower data rate data from said first integrated circuit to said second integrated circuit, said second integrated circuit including a de-serializer to receive said lower data rate data from said first integrated circuit and demultiplex said lower data rate data and said control information before transmitting said data to a device for demodulating said data.

~~24~~²¹ (Original). The modem of claim ~~23~~²⁰ wherein said second integrated circuit includes a modulating circuit which decreases the data rate of digital data and a serializer which transmits said decreased data rate data to said first integrated circuit, said first integrated circuit including a de-serializer that receives said modulated data, said de-serializer coupled to a device that increases the data rate of said data, said device coupled to a digital-to-analog converter.

~~25~~²⁴ (Original). The modem of claim ~~23~~²⁰ wherein said device on said first integrated circuit for decreasing the data rate of said data is a decimation filter.

~~26~~²² (Original). The modem of claim ~~24~~²¹ wherein said device that increases the data rate on said first integrated circuit is an interpolation filter.

~~27~~²³ (Original). The modem of claim ~~24~~²¹ wherein said modulating circuit includes an inverse fast Fourier transformer.

~~28~~²⁵ (Original). The modem of claim ~~23~~²⁰ wherein said modem is a splitterless remote modem.

Claim 29 (Canceled).

~~30~~²⁶ (Original). The modem of claim ~~23~~²⁰ wherein lower data rate data is transmitted in two directions between said first and second integrated circuits.